REMARKS

Claims 1-21 are pending.

Information Disclosure Statement

The Patent Office considered the information disclosure statement submitted by the Applicant.

Claim Rejections – 35 U.S.C. §102

The Patent Office rejected claims 1-3 and 7-9 under 35 U.S.C. §102 as being anticipated by Fujisawa, U.S. Patent 5,086,346 ("Fujisawa").

Applicant respectfully traverses. The present application discloses a novel and nonobvious method and system for employing a FIFO memory with single port memory modules that allow simultaneous read and write operations. Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *W.L. Gore & Assocs. v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). Further, "anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983). Emphasis added.

Applicant respectfully submits claims 1 and 7 recite elements which have not been disclosed, taught or suggested by Fujisawa. For example, claims 1 and 7 generally recite providing a first single port memory module for an even address of an operation and providing a second single port memory module for an odd address of an operation. Fujisawa fails to teach, disclose or suggest providing a first single port memory module for an even address of an operation and providing a second single port memory module for an odd address of an operation. The Patent Office cites FIG. 15 and elements 62, 63 for support of its assertion that Fujisawa recites each element of claims 1 and 7.

However, elements 62 and 63 represent a FIFO line memory which include a separate read clock and write clock. A FIFO line memory with a separate read clock and write clock is not equivalent to a single port memory module as recited in claims 1 and 7. Consequently, elements of claims 1 and 7 have not been disclosed by Fujisawa. Under *Lindemann*, a *prima facie* case of anticipation has not been established for claims 1 and 7. Claims 2-3 and 8-9 are believed allowable due to their dependence upon an allowable base claim.

Claim Rejections – 35 U.S.C. §103

The Patent Office rejected claims 4-6 and 10-12 under 35 U.S.C. §103 as being unpatentable over Fujisawa, U.S. Patent 5,086,346 ("Fujisawa") in view of Microsoft Computer Dictionary.

Applicant respectfully traverses. It is contended that all of the claims rejected under this section depend on independent claims 1 and 7, both of which are non-anticipatory and non-obvious as discussed. Thus, dependent claims 4-6 (which depends on independent claim 1) and dependent claims 10-12 (which depends on independent claim 7) should be allowed.

Allowable Subject Matter

The Patent Office stated claims 13-21 are allowed.

Applicant thanks the Patent Office for the indication of allowed claims. Applicant understood that the reasons for the indication of allowable subject matter given by the Patent Office at Page 5 of the Office Action of March 23, 2006 were made in accordance with the following instruction per MPEP § 1302.14:

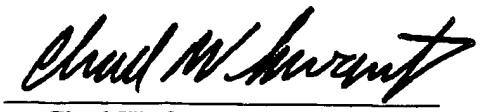
> "The statement is not intended to necessarily state all the reasons for allowance or all the details why claims are allowed and should not be written to specifically or impliedly state that all the reasons for allowance are set forth."

CONCLUSION

In light of the forgoing, reconsideration and allowance of the claims is earnestly solicited.

Respectfully submitted,
LSI Logic, Inc.

Dated: May 11, 2006

By: 
Chad W. Swantz
Reg. No. 46,329

SUITER · WEST · SWANTZ PC LLO
14301 FNB Parkway, Suite 220
Omaha, NE 68154
(402) 496-0300 telephone
(402) 496-0333 facsimile